Development of a Large Area Fast Readout HPC Detector

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The XSPA detectors are designed based on UFXC32k IC [1] designed by AGH University of Science and Technology. Single module consists of 16 UHXC chips tiled on the backside of the monolithic sensor which has 1024 x 512 76 um sq. pixels. No inter-chip pixels in between ROICs which terribly suffer the image quality.

XSPA detector series is aiming not only for X-ray imaging but also for time-resolved X-ray measurements. Dealing with "inter-chip pixels" is our main feature for imaging, and for time-resolved measurements we understand that frame rate is as important as the size of the pixels and the area of the detector. Thanks to UFXC32k IC's high count-rate and fast operation capability, combined with our high data throughput backend circuits, XSPA-1M (consists of two XSPA-500k modules) is capable of more than 50 kfps with continuous exposure (zero-deadtime mode operation with 2-bit counter/pixel.) If the non-continuous exposure (burst-mode operation [2]) is allowed, it can achieve over 970 kfps with ~2 % duty ratio.

In addition, XSPA-1M detector can operate with very short gate time (down to 48 ns / frame) utilized to deal with charge sharing events and for sub-pixel resolution measurements.

[1] P. Grybos et al. IEEE Trans. Nucl. Sci. vol. 63, no. 2, pp. 1155-1161, Apr. 2016.

[2] Q. Zhang et al. J. Synchrotron Rad. vol. 25, pp. 1408-1416, Jun. 2018.