MS44-1-11 Azimuthal integration for fast X-ray area detectors on FPGAs
#MS44-1-11

Z. Matej [1], K. Skovhede [2], C.P. Johnsen [2], A. Barczyk [1], C. Weninger [1], A. Salnikov [1], B. Vinter [2]
[1]MAX IV Laboratory, Lund University - Lund (Sweden), [2]Niels Bohr Institute, University of Copenhagen - København (Denmark)

Abstract
Developments in X-ray detectors and increasing brightness of new generation light sources as X-ray free electron lasers and diffraction limited storage rings allow faster diffraction experiments. In order to catch up with the high data rates and to provide feedback to experiments with the lowest possible latency a compute acceleration of azimuthal integration (AZINT) of scattering data from X-ray area detectors is done here on field-programmable gate arrays (FPGAs). FPGA is a sort of computer chip hosted on a computer board which is often connected directly to external electronic devices as detector readout circuits or network transceivers. Modern “compute” FPGAs can be equipped with large memory and hosted in a computer exactly the same way as graphical processing units (GPUs). Moreover they can be programmed, beside other options, with the same programming language. In particular with OpenCL – the standard programming model used e.g. in the pyFAI azimuthal integration toolbox. OpenCL and synchronous message exchange (SME) were used to implement AZINT on FPGAs and to process data from X-ray diffraction experiments. Compute FPGAs are excellent candidates for processing high throughput detector data. All the tasks of receiving, decompressing the camera image stream and the final AZINT computation can be handled on a single device. The FPGA implementation allows for fixed and extremely short latencies in receiving integrated diffraction patterns that can be fitted in other parts of the configurable pipeline and provide a real-time feedback to the experiment. The solution can be integrated with compute infrastructures at large scale facilities or as an embedded device it can increase capabilities of handling high throughput detector data in any lab. It is available in the DevCloud [1] as well now. It is demonstrated the FPGA implementation can process several (>6) Giga-pixels per second on the mid-range FPGAs. That matches well the maximum frame-rates of detectors at MAX IV nowadays and it is well comparable with capabilities of high-end GPUs.

References
[1] https://gitlab.com/MAXIV-SCISW/compute-fpgas/bincount (last visited, 4 July 2022)