

Development of an ultra-fast data-acquisition system for a two-dimensional microstrip gas chamber

Atsuhiko Ochi,^{a*} Toru Tanimori,^a Yuji Nishi,^a
Shunsuke Aoki^a and Yasuro Nishi^b

^aDepartment of Physics, Tokyo Institute of Technology, Tokyo 152-8551, Japan, and ^bX-ray Research Laboratory, Rigaku Corporation, Tokyo 196-8666, Japan.
E-mail: ochi@tithp0.phys.titech.ac.jp

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A high-performance data-acquisition system has been developed in order to obtain time-resolved sequential images from a two-dimensional microstrip gas chamber (MSGC). This was achieved using fully digital processing with a synchronized pipeline method. Complex logical circuits for processing large numbers of signals are mounted on a small number of complex programmable logic devices. The system is operated with a 10 MHz synchronous clock, and has the capability of handling more than 3×10^6 counts s^{-1} for asynchronous events. The system was examined using a 5×5 cm MSGC and the recently developed 10×10 cm MSGC (1024 outputs); the anticipated performances were achieved.

Keywords: microstrip gas chambers (MSGCs); time-resolved studies; data-acquisition systems.

1. Introduction

The microstrip gas chamber (MSGC) was proposed by Oed (1988) as a new type of gas detector. Detectors of this type are anticipated as a new generation of particle detectors, with fine position resolution and low space-charge effects in comparison with wire-type gas chambers. MSGCs with two-dimensional readout have been developed by our group (Nagae *et al.*, 1992; Tanimori *et al.*, 1992). MSGCs have fine position resolution and a very short dead time for each incident particle; therefore, they are good position-sensitive detectors for high-luminosity X-rays. In particular, MSGCs are expected to be able to observe time-resolved X-ray images using a synchrotron radiation source. Since the construction of third-generation synchrotron radiation facilities, which are now available all over the world, the demand for imaging detectors capable of operation with such brilliant sources has greatly increased.

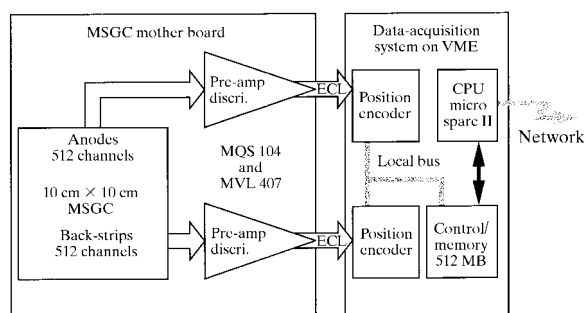


Figure 1
Block diagram for the MSGC data-acquisition system.

Our MSGC with a 200 μm pitch electrode has the following features: (i) fine position resolution of about 100 μm , (ii) high rate capacity for incident X-rays of 10^7 counts $s^{-1} \text{mm}^{-2}$, and (iii) fine timing resolution of ~ 50 ns. The details and recent status of our MSGCs are described by Tanimori *et al.* (1996, 1998). These features of MSGCs may satisfy the demands of many synchrotron radiation experiments. However, one of the most serious problems for an MSGC operated under intense X-rays is limitation of the data-acquisition (DAQ) capability. Generally, more than several tens of thousands of events are necessary to construct two-dimensional images, and frames of a few tenths of a second are required to obtain the image as a movie. Thus, more than 10^6 counts s^{-1} capacity is required for real-time X-ray imaging analysis. With this motivation, a new fast DAQ system has been developed. Such a system is considered to be achievable only by digital-hardware processing under the present technology. Our system was successful in obtaining data from an MSGC at more than 3×10^6 counts s^{-1} . Since an MSGC is a pulse-counting detector, the DAQ system can conserve both positional and timing information of incident photons. Using the timing of each photon, X-ray imaging on a sub-millisecond time scale is possible, and microsecond-order imaging is possible for periodical or reproducible phenomena.

2. DAQ system

Fig. 1 shows a block diagram of the new DAQ system. The large number of signals to be processed from the MSGC makes the new system very complex. In order to process so many signals in a short time, only the discriminated information about a signal ('on' or 'off') is used. The pulse heights of the anodes and back-strips are ignored, although the total charge of one event can be recorded by summing signals induced on cathode strips. The x and y positions of an incident particle are obtained from discriminated input signals by the digital-encoding circuits, and these positions are recorded to DRAM (dynamic random access memory). The DRAM can also be accessed from the system CPU. The system was realized on the 9-unit VME-bus system. The CPU used was a

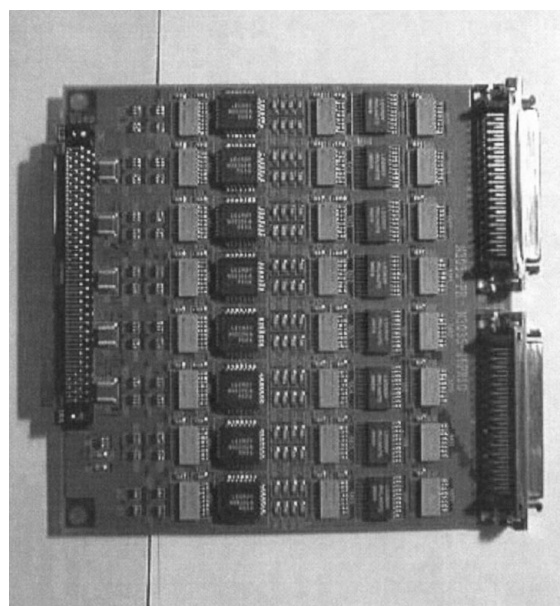


Figure 2
64-channel pre-amplifier board.

FORCE CPU-5V running the UNIX operating system. This CPU controls both the DAQ system and the external network interface.

The DAQ system consists of pre-amplifier cards, position-encoding modules (PEMs), a control and memory module (CMM) and the CPU board.

2.1. Pre-amplifier and discriminator card

Pulses from the anode and back-strip of the MSGC are amplified by fast shaping amplifiers (LeCroy MQS104A) and discriminated by the monolithic comparator (LeCroy MVL407S) on the cards inserted vertically onto the MSGC board. The discriminator pulses are fed by differential ECL standard. The four channel-circuits of both the amplifier and the discriminator are packaged in one IC chip, and 16 sets of these (corresponding

to 64 channels) are mounted on a pre-amplifier card, as shown in Fig. 2. The size of this card is 135 × 147 mm, with a thickness of 15 mm (including the output connectors). For 1024 anodes and back-strips, 16 pre-amplifier cards are used. The MSGC with pre-amplifier cards is shown in Fig. 3. All signals from the anodes and back-strips are processed as one-bit digital data. Using this method, the position resolution would be poor for a multi-wire chamber. However, due to the fine pitch (200 μm), the MSGC provides a position resolution of 100 μm using only digital data.

2.2. Position-encoding module (PEM)

The PEM encodes 1024 bits of signals from the 10 × 10 cm MSGC into 20 bits of position data. The PEM is the most complicated and important part of a fast DAQ, in which all data processing necessary to obtain the hit position is performed by digital hardware, including noise reduction and calculation of the centroid of the cluster of hits. As one PEM handles 256 signals from the MSGC, four modules were needed for the 10 × 10 cm MSGC. Fig. 4 shows two PEM modules and a CMM module. Fig. 5 shows a block diagram of the PEM. The input of ECL-differential standard is translated to TTL standard and fed to encode logic which consists of several complex programmable logic devices (CPLDs). The CPLDs EPM7256E and EPM7192E (Altera Corporation) are used. These CPLDs have a large number of I/O pins (EPM7256 has 160 pins available), enabling the devices to deal with a large number of inputs. The first stage in the signal processing is a synchronization of the input data with the system clock cycle. In the second stage, the positions of the electrodes hit are synchronously encoded. A few sequential strips of the MSGC are usually hit by one incident X-ray. The position of the incident X-ray is determined to be the centre of the electrodes hit. The highest and lowest positions of electrodes hit are calculated by a priority encoder and are averaged to obtain the centre. The validity of signals is also checked in this circuit as follows: events which involve only one cluster of sequential electrodes are taken to be valid events, and those which involve two or more clusters are rejected. The encoding and validity checks are processed by a pipeline method in one stage per clock cycle. The data-processing capacity is ideally one event per clock cycle. The system was operated with a 10 MHz clock cycle, which is soon to be increased to 20 MHz. The details of these methods are described by Ochi (1998).

2.3. Control and memory module (CMM)

The encoded data from the PEMs are fed to the CMM board via a J3 VME bus. The roles of the CMM are data accumulation from the PEMs and interfacing with the CPU. The validity of data is checked when signals come from both anodes and back-strips and there is only one cluster in a clock cycle. The validity (ACCEPT) is judged by the following logical formula,

$$ACCEPT = [(AHIT1 \oplus AHIT2)(AHIT1 \oplus AHIT2)]\overline{DUP}$$

where the event signals from the four encoder boards (two dealing with anodes, the others dealing with back-strips) are AHIT1, AHIT2, BHIT1 and BHIT2, and DUP is signalled when there are two or more clusters. The accepted signal is fed to the storage memory via FIFO (first in first out) memory. In this system, the maximum memory of 512 Mbyte is mounted, and this memory can be accessed from the CPU board by VME bus. Data from one event consist of the x and y positions (20 bit), timing of the data input (4 bit) and the energy information of the incident X-ray

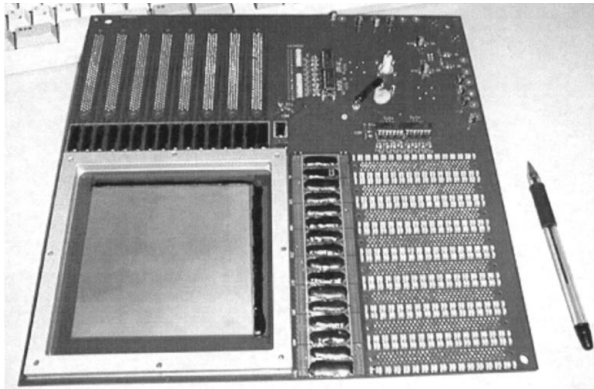


Figure 3
10 × 10 cm MSGC.

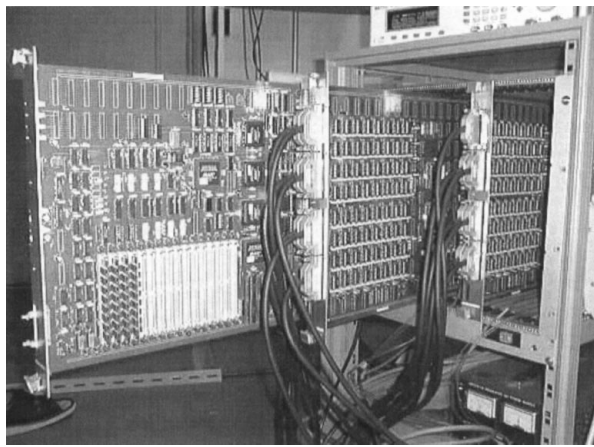


Figure 4
Ultra-fast data-acquisition system.

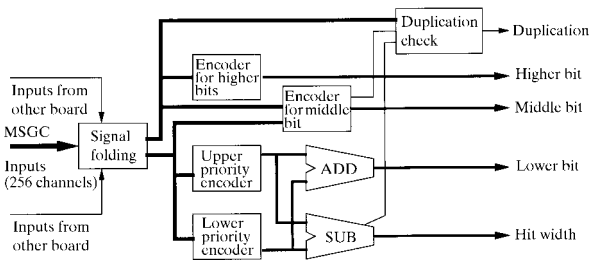


Figure 5
Block diagram for the position encoder.

from the ADC (8 bit). Therefore, a total of 32 bits (4 bytes) are required for one event, and 1.3×10^8 counts are held temporarily.

2.4. CPU board

The CPU board controls the encoding system and the data transfer to other computers *via* a network. In this system, a FORCE CPU-5V on which a microSPARC (110 MHz) CPU is mounted is used due to its interchangeability with a UNIX workstation. In the VME system, the memory on the CMM can be accessed from the CPU in a similar manner to the internal memory of the CPU. The data from the MSGC is therefore processed immediately by the CPU system. It is also possible for the main data analyses to be processed by an external fast CPU linking to the powerful UNIX network facility.

3. Performance of the DAQ system

In order to evaluate the performance of the new DAQ system, static images and sequential images for a moving object were obtained using the 5×5 cm and 10×10 cm MSGCs operated under intense X-rays. Half the system (using two PEM modules) was tested by connecting the 5×5 cm prototype MSGC, and the full system (four PEM modules) was tested using the 10×10 cm MSGC. The details of these MSGCs are described by Tanimori *et al.* (1996, 1998). In all these measurements, X-rays from a tube with a copper target were used. The tube voltage was 20 kV and the intensities of the X-rays were controlled by the tube current (2–30 mA) and beam dumpers made of 100 μ m copper foil. The relative X-ray intensity was measured by the counting rate of the MSGC itself at low intensity and extrapolated at high intensity using the relation between the thickness of the beam dumper and the tube current of the generator at high intensity. X-rays from the generator were emitted in the region of 1 msrad. This solid angle corresponds to a spot of 12 cm diameter at a distance of 1 m from the source. To test the imaging performances, transmission images were taken.

Fig. 6 plots the number of events handled by the DAQ system *versus* the relative X-ray intensity. The number of events handled by the DAQ system increases linearly up to 10^6 counts s^{-1} and gradually saturates approaching 3×10^6 counts s^{-1} . The maximum number of counts achieved was 3.2×10^6 counts s^{-1} . This shows

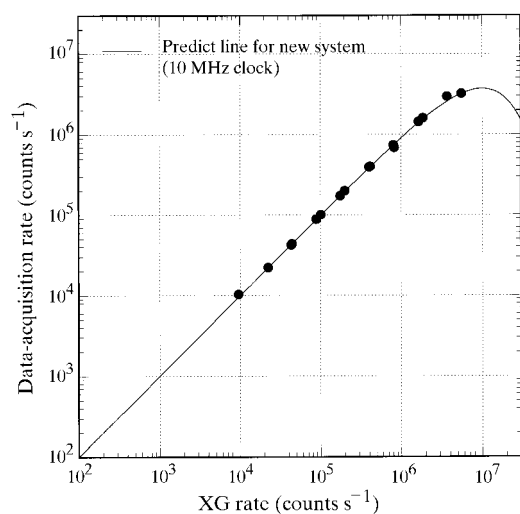


Figure 6
Results of the DAQ rate performance test.

that the system has the capacity to process 10^6 events s^{-1} for synchronous events. However, X-rays usually enter the MSGC randomly, and a duplication hit in one cycle decreases the capability. The probability of a number of event counts occurring in one cycle is determined by a Poisson distribution, and the case of one event per cycle is processed as a valid event. Therefore, the expected DAQ rate R is calculated by

$$R(r) = r \exp -r/c,$$

where r is the pulse-counting rate of the MSGC, which is proportional to the X-ray intensity, and c is the clock cycle. The maximum value of $R(r)$ is c/e when $r = c$, giving a theoretical limit of about 3.7×10^6 counts s^{-1} for the system. Our results are consistent with this limit.

Fig. 7(a) shows the transmission image of a small metal pendant obtained using the MSGC and DAQ system. The exposure time was about 8 s, and 5.9×10^5 X-ray events were obtained. An image with the same exposure time using the old system is shown in Fig. 7(b) for comparison. Only 1000 events are used for this

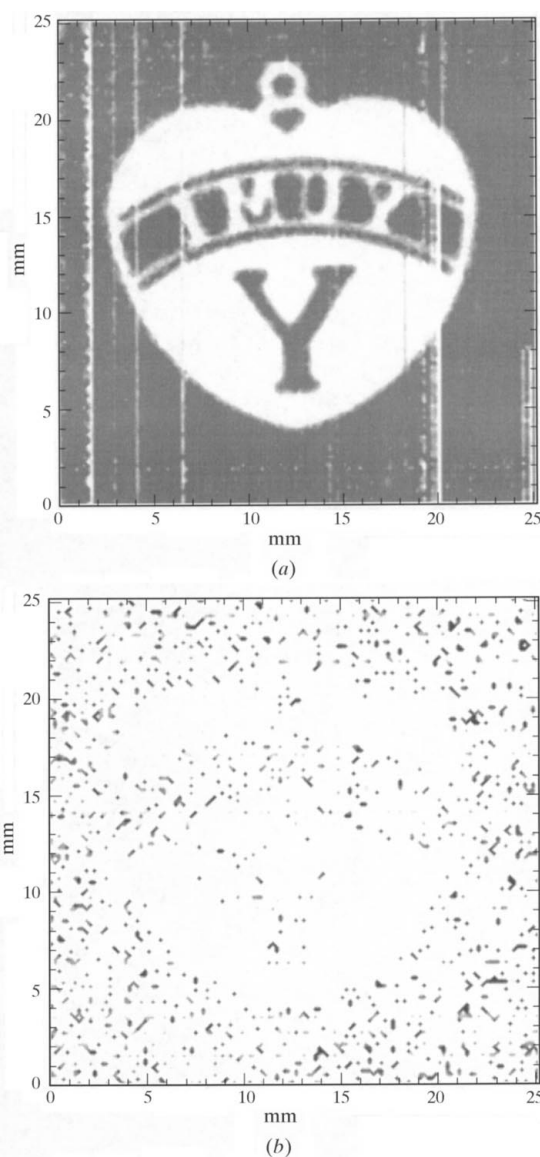


Figure 7
Imaging capacity for 8 s exposure time with (a) the newly developed data-acquisition system and (b) the old data-acquisition system.

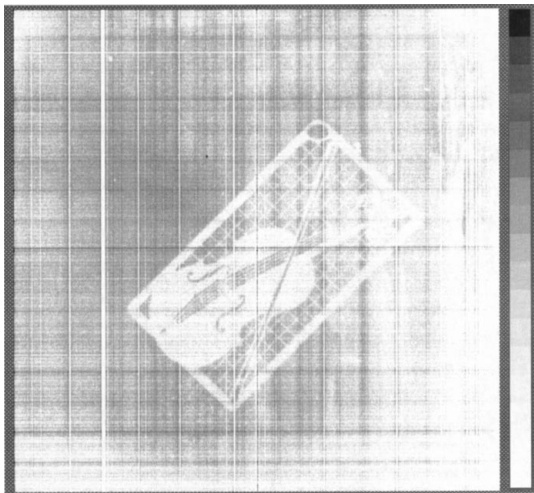


Figure 8

X-ray transmission image using a 10×10 cm MSGC. As the electronics had not been tuned, some horizontal and vertical stripes were observed.

image formation. With a sufficient number of events, the position resolution is about $100 \mu\text{m}$. The most detailed structure of the pendant ($\sim 200 \mu\text{m}$) is observed clearly in Fig. 7(a). X-ray imaging using the 10×10 cm MSGC with the full set-up was also successful. Fig. 8 shows the transmission image of a violin-shaped metal bookmark.

The imaging performance for a moving object was tested by obtaining the transmission image of a rotating metal pendant. The rotation speed was about $1 \text{ rotation s}^{-1}$. X-rays of $1.3 \times 10^6 \text{ counts s}^{-1}$ intensity were used for this measurement. Fig. 9 shows snapshots for each 20 ms acquisition time. The series of images can be displayed continuously. As the data from this system contain a time stamp of microsecond order, imaging of this order is available for the observation of periodical phenomena.

4. Summary

A fast data-acquisition system for the MSGC has been developed. The system has 1024 input channels, and the input signals are processed as purely digital signals. The input signals are synchronized to a 10 MHz clock cycle, and for each cycle, signals are encoded to the digital position using a pipeline method. The validity of each signal is checked and all valid signals are stored in the memory of the CMM, which is accessible from the CPU. The performance of the system was checked using the MSGC operated under highly intense X-rays. A large handling of $3.2 \times 10^6 \text{ counts s}^{-1}$ was achieved as the maximum data-acquisition rate, and is approximately equal to the theoretical limit with a 10 MHz clock.

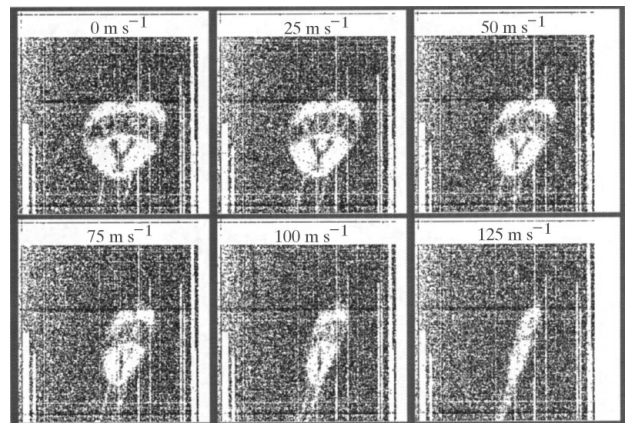


Figure 9

Snapshots of the X-ray transmission image of a moving object.

The X-ray imaging had $\sim 100 \mu\text{m}$ position resolution, and a moving picture of the X-ray transmission image (50 frames s^{-1}) was successfully obtained.

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